Amendments to the Specification

Please amend the second and third paragraphs on page 6 as follows:

In the second embodiment, in a diffusion bit array of the twin MONOS memory where the memory device structure is fabricated as described in U.S. Patent 6,248,633 B1, the bit diffusion contact for stitch151 is formed. Then by utilizing the resistive to conductive layer stitching method which was described in the first embodiment scheme, the control gate polysilicon 143 is stitched with Metal 1 (161) and at the line edge, as shown in ~~FIG~~Fig. 5B. In the array, metal 2 (M2) 171 is used to lower the resistance of the polysilicon word gate line. However, in the stitch area, as demonstrated in ~~FIG~~Fig. 5C, M2 172 is also used to connect the edges of the severed CG lines that are contacted to Metal 1 (M1) 161. The M2 line loops around the contact/via stack 151, which connects the diffusion bit line103 to the parallel running Metal 3 181 in Fig.5D. Since the loop of M2 171 blocks the bit line contact in the adjacent cell, the stitch region contacts alternate bit lines and alternate CG lines. The uncontacted set of lines may be stitched immediately below in a separate stitch area or at the other end of the sub array. It is also possible to interchange the functions of metal 1 and metal 2 for this array, such that metal 1 is used to contact to the word line and for the stitch loop, and metal 2 is used to stitch to and reduce the resistance of the control gate line.

In the third embodiment of this invention, the stitching method also incorporates a bit diffusion select transistor and/or a control gate line select transistor. The purpose of the select transistors may be to reduce the overall capacitance of the bit line or control gate line, or to limit the disturb conditions that a grouped sub-array of cells may be subjected to during program

and/or erase. These select transistors are added into the stitch areas between memory cell sub-arrays. ~~FIG~~Fig. 8A and Fig.9C show an implementation example of a bit line select gate 211 and control gate select gate 212 in the stitch area. Referring to ~~FIGS~~Figs.7A-E and 8A, the stitch areas on both sides of a sub-array are shown. Bit line select gates 211 are placed closest to the array and the control gate select gates 212 are placed outside of the bit line select gates from the array. At the end of the sub-array, the bit diffusion is extended past the edge of the control gate by implanting N+ species such as As prior to formation of control gate sidewalls (Fig.9A). The bit diffusion extension 204 and bit select transistors 211 are provided alternatively on both sides of the sub-array. Select transistors are isolated from each other by shallow trench isolation. (Fig.7E and Fig.8A) The bit select gate 211 is placed horizontally across the extended bit diffusion and the horizontal gate becomes the bit select gate. The diffusion on the other side of the bit select transistor gate is connected to the main bit line by a contact stack 251 between the diffusion to second level metal 2 (271) as shown in Fig.9A. When control gate select transistors 212 are also needed, a pair of control gate select transistors 212 are placed out of phase, and between the two bit line select transistors 211 inside the two edges of two sub-arrays. The pair of control gate select lines run parallel to the word gate and perpendicular to the bit line and control gate lines (Fig.8A). The center contact 254 between two control gates 212 becomes the control gate connection point to the main control gate line which runs vertically in metal M3 (281), as illustrated in Figs.8A and 8D. The other diffusion region of the control gate select transistor is locally connected by metal M1 (261) to the other end of the polysilicon control gate stitch 252. (Fig.8B) Main bit lines run in metal 2 (271), but near the main CG contact, they are cut and connected down to metal 1 (261), in order to loop around the main control gate contact 254 to complete the bit stitch (Fig.8C). Thus at the one edge of sub-array space, alternative bit select gate/stitch via M2 line and control gate select/stitch via M3 may be completed using a M1-local connection and loop. Metal 1 may also be used in the array region to stitch the word gate lines at intervals to reduce the polysilicon word gate resistance. This

example shows a bit select transistor and control gate select transistor. Using the same contact and metal wiring approach, it is also possible to implement the stitch and select area with transistors for only bit line selection or with transistors for only control gate line selection.